WHAT IS CLAIMED IS:

1. An output driver comprising:

an output multiplexor receiving a data signal and outputting a q-node signal; and

an output current driver having a plurality of transistor stacks wherein each transistor stack is responsive to a current control signal that enables the q-node signal to cause a predetermined amount of current to flow through the transistor stack thereby adjusting the output drive current.

2. The output driver of claim 1 wherein at least one of the transistors in each transistor stack is a binary weighted device with respect to at least one other transistor in another transistor stack.

3. The output driver of claim 1 wherein a transistor stack comprises two transistors and the current control signal connects to the gate of one of the transistors, and the q-node signal connect to the gate of the other transistor.

4. The output driver of claim 1 wherein the transistors are n-type transistors.

5. The output driver of claim 3 wherein the transistors connecting to the current control signals have a positive threshold voltage in the range of about 0.3 to 0.4 volts.

6. The output driver of claim 1 wherein:

the output current driver has an output drive transistor with a predetermined threshold voltage, the output drive transistor being responsive to the q-node signal; and wherein

the output multiplexor outputs a q-node signal to the output drive transistor wherein the q-node signal is regulated to a maximum predetermined value such that the output drive transistor operates in saturation when outputting a predetermined low level bus output voltage.

7. The output driver of claim 6 wherein:

the maximum predetermined value of the q-node signal is substantially equal to the predetermined threshold voltage plus the predetermined low level bus output voltage.

8. An output driver comprising:

an output multiplexor for receiving a data signal and outputting a q-node signal on a q-node output line, the output multiplexor having a base block and at least one slew rate adjustment block connected in parallel with the base block, each slew rate adjustment block having a control block and a stacked transistor pair connected in series with the control block, the control block being responsive to a slew rate control signal that enables the stacked transistor pair to be responsive to the data signal, the outputs of the plurality of the stacked transistor pairs being connected in parallel to a q-node output line; and

an output current driver for outputting a data bus signal with a predetermined output drive current in response to the q-node signal.

9. The output driver of claim 8 wherein the stacked transistor pair comprises a p-type transistor connected in series with an n-type transistor.

10. The output driver of claim 9 wherein the control block further comprises a NAND gate and a NOR gate, the NAND gate for enabling the p-type transistor, and the NOR gate for enabling the n-type transistor.

11. The output driver of claim 8 wherein the base block, control block and stacked transistor pair connect to a predriver power line having a V-gate voltage different from a supply voltage, wherein the V-gate voltage causes an output transistor of the output current driver to operate in saturation when driving a low voltage level.

12. An output driver comprising:

an output multiplexor including a predriver for receiving a data signal and outputting a q-node signal on a q-node output line, also including a kickdown circuit, the predriver being supplied with a high level voltage and a low level voltage, the pre-driver for driving the q-node signal between the high level voltage and the low

level voltage, the kickdown circuit also receiving the data signal and q-node signal and for increasing the rate at which the q-node signal transitions to the low level voltage; and

an output current driver responsive to the q-node signal outputting a data bus signal with a predetermined output drive current.

13. The output driver of claim 12 wherein the kickdown circuit includes a stacked transistor pair, one transistor of the stacked transistor pair being responsive to the data signal, the other transistor of the stacked transistor pair being responsive to the q-node signal, such that when the data signal is at a low level and the q-node signal is transitioning from a high level to the incoming low level, both transistors of the kickdown circuit are conducting current thereby driving the q-node signal on the q-node line to the low level.

14. An output driver comprising:

an output multiplexor including a predriver for receiving a data signal and outputting a q-node signal on a q-node output line, the predriver being supplied with a high level voltage and a low level voltage, the pre-driver for driving the q-node signal between the high level voltage and the low level voltage;

a duty cycle compensator receiving a clocked data signal and outputting the data signal to the predriver, the duty cycle compensator modifying the duty cycle of the clocked data signal in response to at least one slew rate control bit; and

an output current driver responsive to the q-node signal outputting a data bus signal with a predetermined output drive current.

15. The output driver of claim 14 wherein the predriver distorts the duty cycle of the data signal by a predetermined amount, and the duty cycle compensator modifies the duty cycle of the clocked data signal with respect to the predetermined amount such that the Vout signal output by the output driver has no distortion.

16. The output driver of claim 14 wherein the duty cycle compensator further comprises at least one stacked transistor pair that is enabled by the at least one slew rate control bit, such that when the clocked data is transitioning from a high level to a

low level the duty cycle compensator causes the data signal to transition from a high to a low at an earlier point in the duty cycle than would otherwise occur.

17. An output driver comprising:

an output current driver having an output drive transistor having a predetermined threshold voltage and an output impedance; and

an output multiplexor receiving a data signal and outputting a q-node signal to the output drive transistor wherein the output impedance is maintained within a predetermined range when the output drive transistor is outputting a low voltage level.

18. The output driver of claim 17 wherein the output impedance exceeds 150 ohms.

19. An apparatus for maintaining an output impedance of an output driver within a predetermined range, comprising:

a predriver for receiving a data signal and outputting a q-node signal to the output driver, such that the q-node signal transitions between a low voltage level and a high voltage level; and

a v-gate supply for supplying power to the predriver and causing the high voltage level of the q-node signal to be substantially equal to a predetermined v-gate voltage to maintain the output impedance of the output driver above a predetermined threshold when the output driver is outputting a low voltage level.

20. The apparatus of claim 19 wherein the predetermined v-gate voltage is substantially equal to a predetermined threshold voltage of the output driver plus the low voltage level output by the output driver.

21. The apparatus of claim 19 wherein the predetermined threshold is about 150 ohms.

22. The apparatus of claim 19, further comprising:

a charge compensator for maintaining the high voltage level of the q-node signal at the v-gate voltage wherein a predetermined amount of charge is delivered to the v-gate voltage based on the data signal.

23. The apparatus of claim 22, further comprising:

a charge compensation bit generator for generating a compensation signal, wherein the predetermined amount of charge delivered by the charge compensator is also based on the compensation signal.

24. An output driver comprising:

an input block for multiplexing an odd data signal and an even data signal with a clock signal to output a clocked data signal;

a duty cycle compensator for receiving the clocked data signal and outputting a precompensated clocked data signal with a duty cycle that is changed by a predetermined amount;

a predriver for generating a q-node signal based on the precompensated clocked data signal, the q-node signal transitioning between a low voltage level and a high voltage level at a predetermined slew rate, such that the Vout signal has the same duty cycle as the clocked data signal; and

a kickdown circuit responsive to the precompensated clocked data signal and the q-node signal, for increasing the rate of transition of the q-node signal from a high voltage level to a low voltage level;

a V-gate generator for causing the high voltage level of the q-node signal to be substantially equal to a predetermined V-gate voltage;

a charge compensator for maintaining the high voltage level of the q-node signal at the V-gate voltage wherein a predetermined amount of charge is delivered to the V-gate voltage based on the precompensated clocked data signal;

a charge compensation signal generator for generating a compensation signal, wherein the charge compensator delivers the predetermined amount of charge based on the compensation signal; and

an output current driver, responsive to at least one current control bit and to the q-node signal, for outputting a data bus signal.

25. The output driver of claim 24 wherein the V-gate generator causes the high voltage level of the q-node signal to be substantially equal to the predetermined V-gate voltage for a range of supply voltages.

26. A method for outputting data signals to a bus from an integrated circuit, comprising the steps of:

receiving a data signal having a duty cycle;

precompensating the data signal by changing the duty cycle by a predetermined amount;

modifying the slew rate of the precompensated data signal by a predetermined amount to generate a q-node signal; and

increasing the rate of transition of the q-node signal from a high voltage level to a low voltage level based on the precompensated data signal and the q-node signal.

27. The method of claim 26 further comprising the step of:

generating a V-gate voltage having a lower voltage level than a supply voltage, wherein the high voltage level of the q-node signal is substantially equal to the V-gate voltage.

28. The method of claim 27, further comprising the steps of:

delivering a predetermined amount of charge to the V-gate voltage based on the precompensated data signal.

29. The method of claim 28, further comprising the steps of:

delivering the predetermined amount of charge to the V-gate voltage based on a compensation signal.